ON-CHIP DEAD PIXEL CORRECTION IN A CMOS IMAGING SENSOR

Field of the Invention

The present invention relates to metal oxide semiconductor (MOS) imaging arrays and, more particularly, to a method for correcting for dead pixels in MOS imaging arrays.

Background of the Invention

Integrated circuit technology has revolutionized various fields including computers, control systems, telecommunications, and imaging. In the field of imaging, the charge coupled device (CCD) sensor has made possible the manufacture of relatively low-cost and small hand-held video cameras. However, the solid-state CCD integrated circuits needed for imaging are relatively difficult to manufacture, and therefore are expensive. In addition, because of the differing processes involved in the manufacture of CCD integrated circuits relative to MOS integrated circuits, the signal processing portion of the imaging sensor has typically been located on a separate integrated chip. Thus, a CCD imaging device includes at least two integrated circuits: one for the CCD sensor and one for the signal processing logic.

An alternative low-cost technology to CCD integrated circuits is the metal oxide semiconductor (MOS) integrated circuit. Not only are imaging devices using MOS technology less expensive to manufacture relative to CCD imaging devices, for certain applications MOS devices are superior in performance. For example, the pixel elements in a MOS device can be made smaller and therefore provide a higher resolution than CCD image sensors. In addition, the signal processing logic necessary can be integrated alongside the imaging circuitry, thus allowing for a single integrated chip to form a complete stand-alone imaging device.

Examples of MOS imaging devices are detailed in "A ¼ Inch Format 250K Pixel Amplified MOS Image Sensor Using CMOS Process" by Kawashima et al., IEDM 93-575 (1993), and "A Low Noise Line-Amplified MOS Imaging Devices" by Ozaki et al., *IEEE Transactions on Electron Devices,* Vol. 38, No. 5, May 1991. In addition, U.S. Patent No. 5,345,266 to Denyer titled "Matrix Array Image Sensor Chip" describes a MOS image sensor. The devices disclosed in these publications provide a general design approach to MOS imaging devices.

The primary building block of an image formed by an MOS imaging device is a pixel. The number, size, and spacing of the pixels determine the resolution of the image generated by the imaging device. The pixels of a MOS imaging device are semiconductor devices that transform incident light photons into current signals at an array cell, which may be a diode or gate cell. The signal produced by each pixel is generally extremely small, in the nanoampere range.

Although generally quite reliable, the pixels may from time to time exhibit anomalous behavior. For example, if the array cell of the pixel has a defect in its PN junction, it may generate current leakage paths, thus causing the cell site to appear as a white spot in the image signal. The pixel of such a cell site may be referred to as a "dead pixel." The number of dead pixels on a CMOS image sensor is dependent on the quality of the process used for forming the image sensor. In a high resolution sensor that has one million or more pixels, a number of dead pixels invariably result.

The present invention is directed to a method and apparatus that compensates for the foregoing and other problems of the prior art. More specifically, the present invention is directed to a method and apparatus for correcting for dead pixels in a CMOS image sensor.

Summary of the Invention

A method for correcting for dead pixels in a CMOS image sensor is disclosed. According to the method, when the image sensor is first powered on, the pixel array is examined for dead pixels and the locations of any dead pixels that are found are digitally stored. Thereafter, as a given frame of the image sensor is scanned out, the location of the pixels in the frame are compared to the stored locations for dead pixels, and if a dead pixel is determined, the dead pixel signal is compensated for. One method of compensating for a dead pixel signal is to replace it with the pixel signal from a previous pixel, or an average of the previous and following pixels.

Brief Description of the Drawings

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIGURE 1 is a schematic diagram of a pixel array of a CMOS imaging sensor;

FIGURE 2 is a schematic diagram illustrating a pixel referencing scheme for a matrix of pixels of a CMOS imaging sensor;

FIGURE 3 is a block diagram of a CMOS imaging sensor including dead pixel correction circuitry formed in accordance with the present invention;

FIGURE 4A is a flow diagram illustrating the initial dead pixel determination and location storage method of the present invention; and

FIGURE 4B is a flow diagram illustrating the image signal processing and dead pixel correction method of the present invention.

Detailed Description of the Preferred Embodiment

With reference to FIGURE 1, an architecture for a CMOS imaging array 101 includes a rectangular matrix of pixels 103. The number of pixels in the horizontal or x-direction and the number of pixels in the vertical or y-direction constitute the resolution of the imaging array 101. Each of the pixels 103 in a vertical column routes its signal to a single charge amplifier 105.

The retrieval of information from the pixels 103 follows the well-known raster scanning technique. In particular, a row of pixels 103 is scanned sequentially from left to right. The next row is then scanned in this manner until all rows have been scanned sequentially from top to bottom. At the end of each complete scan of the entire array 101, a vertical blanking period of predetermined time occurs until the raster scanning pattern is repeated. This type of scanning follows the NTSC scanning scheme. Control circuitry of conventional design is operative to sequentially read the pixels 103 in this manner.

As each pixel is scanned, the signal from that pixel is provided to the charge amplifier 105 for that column. Thus, the charge amplifiers 105 receive signals sequentially. The sequential signals from the charge amplifiers 105 are then forwarded to a second-stage amplifier 107, which amplifies the signals so that they may be further processed.

FIGURE 2 illustrates a schematic representation of a pixel referencing scheme for referencing the pixels of the pixel array. As seen in the example of FIGURE 2, the referencing scheme is a matrix having dimensions of 240 x 360. It will be understood that much larger matrixes may be used, and that the matrix shown in FIGURE 2 is for purposes of illustration only. Each coordinate of the matrix P(i,j) corresponds to a pixel. For purposes of the present invention, subscripts "i" and "j" are used to identify the particular pixel in the frame.

FIGURE 3 illustrates a block diagram of a CMOS image sensor with circuitry for correcting for dead pixels according to the present invention. As illustrated in FIGURE 3, the CMOS image sensor 100 includes a cell array 101 that outputs pixel signals on lines 108 to signal processing circuitry 110. Signal processing circuitry 110 outputs initial dead pixel processing signals on lines 115 to a dead pixel comparator 120, and thereafter outputs normal image processing signals on lines 118. Dead pixel comparator 120 outputs dead pixel location signals on lines 125 to location storage circuitry 130. Location storage circuitry 130 outputs dead pixel location signals on lines 135 to a location comparator 140. Location comparator 140 outputs dead pixel indication signals on lines 145 to signal processing circuitry 110. A location shift register 150 outputs location signals on lines 153 to location storage circuitry 130, outputs location signals on lines 155 to location comparator 140, and also outputs location signals on lines 158 to cell array 101.

The circuitry of FIGURE 3 generally operates in the following manner. When the CMOS image sensor 100 is first turned on, or is otherwise initialized, location shift register 150 indicates digital pixel coordinates (according to location storage numbers that correspond to a referencing scheme such as that shown in FIGURE 2) as the pixel signals from cell array 101 are read out by signal processing circuitry 110. As will be described in more detail below, if an EPROM storage circuit or similar device is not used to store the dead pixel locations, the dead pixels will need to be scanned each time the image sensor is powered on. To determine the location of any dead pixels during the initialization phase, the signal processing circuitry 110 initially provides the first set of pixel signals to dead pixel comparator 120. A detailed description of one manner in which the dead pixel comparator 120 may operate is described in a pending U.S. patent application titled "Method for Correcting False Spikes in a MOS Imaging Array," Serial No. 08/747,902, filed November 14, 1996, which is commonly assigned and hereby incorporated by reference.

In the present invention, the general process for determining dead pixels is to first precharge the cell array 101 with a fixed voltage. Then the entire array is shielded from light, and the pixels of the array are read sequentially by the signal processing circuitry 110. During this process, the dead pixel comparator 120 determines if each pixel is a dead pixel. When a dead pixel is determined, its location from location shift register 150 is then digitally stored in location storage circuitry 130. Once the entire cell array 101 has been read out, all of the dead pixel locations will have been determined and stored in location storage circuitry 130.

After the initial dead pixel location process is complete, normal image processing can begin. During normal image processing, location shift register 150 indicates digital pixel location numbers (corresponding to a referencing scheme such as that shown in FIGURE 2) as the pixel signals from cell array 101 are read out to signal processing circuitry 110. Location shift register 150 also outputs the current pixel location number to location comparator 140. Location comparator 140 compares the current pixel location number to see if it matches a dead pixel location number as stored in location storage circuitry 130. If location comparator 140 determines that the current pixel corresponds with a dead pixel location, then location comparator 140 outputs a dead pixel indication signal to signal processing circuitry 110.

Signal processing circuitry 110 receives the pixel signals from each pixel of the array 101, and as each pixel is read out, the signal processing circuitry 110 determines whether a dead pixel indication signal is being received from location comparator 140. If the signal processing circuitry 110 does not receive a signal from location comparator 140 indicating that the current pixel being processed corresponds to a dead pixel, then signal processing circuitry 110 outputs the pixel signal as part of the normal image signal on lines 118. If, however, the signal processing circuitry 110 receives a signal from the location comparator 140 that indicates that the current pixel being processed does correspond to a dead pixel, then the signal processing circuitry 110 instead compensates for the signal from the dead pixel.

In the preferred embodiment, the signal processing circuitry 110 may compensate for a dead pixel by repeating the pixel signal from the previously read out pixel. The signal from the previous pixel is easily repeated because it is still contained in signal processing circuitry 110 from the previous pixel processing. In addition, more complex compensation methods may also be used, such as replacing

the dead pixel value with an average of the previous and following pixel values. Also, in some embodiments, an external storage circuit may make more memory available to store large dead pixel location storage numbers.

FIGURES 4A and 4B are flow diagrams illustrating the general method of operation for the circuitry of FIGURE 3. As shown in FIGURE 4A, the initial dead pixel location process begins at a point "A." At a block 200, after the image sensor is powered on or otherwise initialized, the first pixel of the matrix is read out. At a block 202, a determination is made as to whether the pixel is a dead pixel. If the pixel is a dead pixel, the routine proceeds to a block 204, and if the pixel is not a dead pixel, the routine proceeds to a decision block 206. At block 204, the digital location of the dead pixel is stored, after which the routine proceeds to decision block 206.

At decision block 206, a determination is made as to whether the last pixel of the frame has been reached. If the last pixel of the frame has not been reached, then the routine proceeds to a block 208 where the routine increments to the next pixel of the frame, and returns to block 200 to read the next pixel from the pixel array. If the last pixel of the frame has been reached, then the routine proceeds to point "B," where normal signal processing may begin as described below for FIGURE 4B.

As shown in FIGURE 4B, from a point "B," the routine proceeds to block 250 where the incrementing is reset to the first pixel of the matrix. At a block 252, the pixel signal is read out from the pixel array. At a decision block 254, the routine determines whether the pixel location corresponds to the stored location of a dead pixel. If the pixel location corresponds to the stored location of a dead pixel, then the routine proceeds to a block 256, and if the pixel location does not correspond to the stored location of a dead pixel, then the routine proceeds to a block 258. At block 256, the routine compensates for a dead pixel by repeating the prior pixel signal as part of the image signal, and then proceeds to a decision block 260. At block 258, the routine processes the pixel signal as part of the normal image signal.

At decision block 260, the routine determines whether the last pixel of the frame has been reached. If the last pixel of the frame has not been reached, then the routine proceeds to block 262 where the routine increments to the next pixel, and then returns to block 252 for reading out the next pixel from the matrix. If at decision block 260 the routine determines that the last pixel of the frame has been

reached, then the routine returns to block 250 to reset the location increment to the first pixel of the matrix.

The method of the present invention is advantageous over previous methods which did not digitally store the locations of dead pixels and which therefore had to determine the dead pixels every time the pixel array was read out. Thus, through use of the present invention the stored dead pixel locations only need to be determined once during the initial location process and can be corrected for thereafter during normal signal processing. This process is faster and more efficient, as less signal processing is required to determine the dead each time the pixel array is read out.

In addition, all of the circuitry shown in FIGURE 3 may be fabricated as part of a single chip for the CMOS image sensor 100. As illustrated in FIGURE 3, relatively simple processing circuitry allows for relatively small location storage circuitry 130 to be used, in that only the locations of the dead pixels need to be stored. Thus, the chip size of the CMOS image sensor 100 can be kept small while using the dead pixel correction method of the present invention. However, it will be understood that the location storage circuitry 130 could also be implemented in an off-chip format, such as through an external EPROM. Using an external EPROM, more memory would generally be available and more complicated system designs for the method of the present invention could be used. In addition, these types of memory could allow the dead pixel locations to remain in storage even when the image sensor was powered off, thus not requiring the initial dead pixel location process to be repeated every time the image sensor was powered on. However, it will also be understood that the dead pixel location process may be repeated at any time to update the dead pixel locations that are stored.

While the preferred embodiment of the invention has been illustrated and described, it will be appreciated that various changes can be made therein without departing from the spirit and scope of the invention. The present invention has been described in relation to a preferred embodiment and several variations. One of ordinary skill after reading the foregoing specification will be able to effect various other changes, alterations, and substitutions of equivalents without departing from the broad concepts disclosed. It is therefore intended that the scope of the letters patent granted hereon be limited only by the definition contained in the appended claims and equivalents thereof, and not by limitations of the embodiments described thereof.